Assignment #5 – Digital Logic Design I – Combinational Logic

CDA 3100, Computer Organization I

Problem 1 (40 points) Design a circuit that takes three bits X2, X1, X0, as input, and output one bit O as output. O is 1 if and only if 2<=X<=5 when X=(X2, X1, X0) is read as an unsigned integer.

(a) Complete the truth table.

X2	X1	X0	O
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(b) Write down the sum-of-product form of the function without any simplification in the format as: O = (X2 & X1 & X0) | (~X2 & X1 & X0) | … (this is NOT the answer).

O =

(c) Simplify the circuit using Karnaugh-map.

X2X1 / X0	00	01	11	10
0				
1				

(d) Write down the Verilog module for this circuit called module HW5P1 (X2, X1, X0, O).

(e) A Verilog code has been provided for this homework with an empty HW5P1 module. Please replace this module with your module and run simulation. Copy and paste the waveform **only related to this problem** here. One way to copy and paste is: 1) print screen, 2) paste the screen to the windows paint program, 3) crop the waveform, and 4) paste it here.

Problem 2 (40 points) Design a circuit that takes three bits A, B, S as input, and output one bit O as output. If S=0, O=A|B. If S=1, O=A&B.

(a) Complete the truth table.

S	A	B	O
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(b) Write down the sum-of-product form of the function without any simplification in the format as: O = (A &B&S) |(A &B&~S) | … (this is NOT the answer)

O =

(c) Simplify the circuit using Karnaugh-map.

SA / B	00	01	11	10
0				
1				

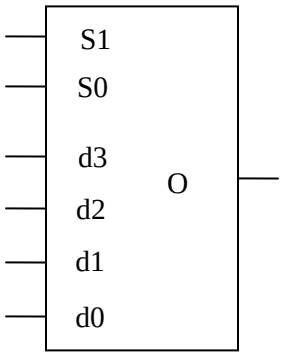
(d) Write down the Verilog module for this circuit called module HW5P2 (S,A,B,O).

(e) A Verilog code has been provided for this homework with an empty HW5P2 module. Please replace this module with your module and run simulation. Copy and paste the waveform **only related to this problem** here.

Problem 3 (10 points) Design a comparator which has 6 input bits, A2, A1, A0 and B2, B1, B0, and one output bit O. Let A=(A2, A1, A0) and B=(B2, B1, B0), and regard them as unsigned integers. If A>B, O=1; else O=0. **Please write down the logic function as your answer. No Verilog code or simulation is needed.** Hint: This problem should be solved by analyzing the underlying logic and no Karnaugh-map is needed. For example, if A2=1 and B2=0, O must be 1 and there is no need to check the values of other input bits.

Problem 4 (10 points) We talked about multiplexors in the class. A 4-1 multiplexor has 6 inputs S1, S0, d3, d2, d1, and d0, and has one output O. It works as follows. If S1S0=00, O=d0. If S1S0=01, O=d1. If S1S0=10, O=d2. If S1S0=11, O=d3. Show how to use **only** one 4-1 multiplexor to implement function F(A,B,C) with truth table shown below. No any other gates should be used, including the inverter; meaning that the inputs to the 4-1 multiplexor can only be from A, B, C, 0, or 1. **Please finish the following figure, showing each input of the 4-1 multiplexor is connected to which one among A, B, C, 0, or 1, as your answer.** No Verilog code or simulation is needed. For this problem, no Karnaugh-map is needed.

A	B	C	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



The Verilog code that will be needed in this homework is:

http://ww2.cs.fsu.edu/~dennis/cda3100_summer_2013/homework/hwk5.v

Instructions about the Verilog Simulator can be found in slides Week8-day1.