

# Assignment #5 – Digital Logic Design I – Combinational Logic

CDA 3100, Computer Organization I

**Problem 1 (40 points)** Design a circuit that takes three bits X2, X1, X0, as input, and output one bit O as output. O is 1 if and only if  $2 \leq X \leq 5$  when  $X = (X2, X1, X0)$  is read as an unsigned integer.

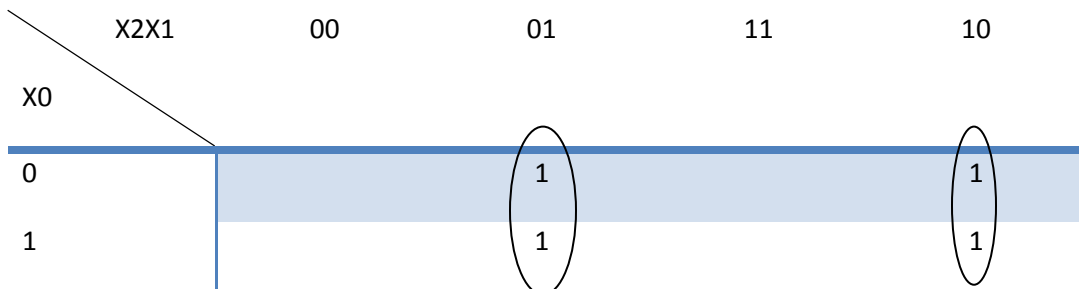
(a) Construct the truth table.

X2	X1	X0	O
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

(b) Write down the sum-of-product form of the function without any simplification in the form as:  $O = (X2 \& X1 \& X0) \mid (\sim X2 \& X1 \& X0) \mid \dots$  (this is NOT the answer).

$$O = (\sim X2 \& X1 \& \sim X0) \mid (\sim X2 \& X1 \& X0) \mid (X2 \& \sim X1 \& \sim X0) \mid (X2 \& \sim X1 \& X0)$$

(c) Simplify the circuit using K-map.



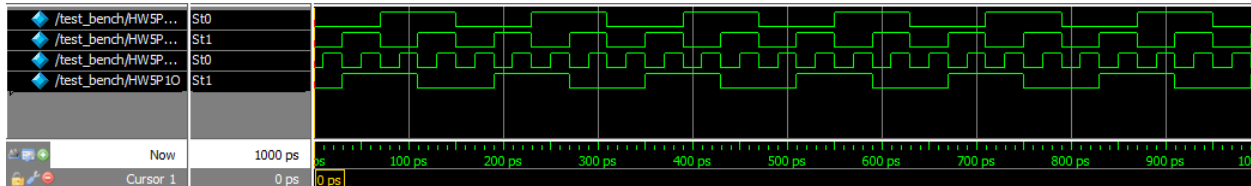
(d) Write down the Verilog module for this circuit called module HW5P1 (X2, X1, X0, O).

```

module HW5P1 (X2, X1, X0, O);
    input X2, X1, X0;
    output O;
    assign O = (~X2&X1)|(X2&~X1);
endmodule

```

(e) \*\*\*\*A Verilog code has been provided for this homework with an empty HW5P1 module. Please replace this module with your module and run simulation. Copy and paste the waveform **only related to this problem** here. (One way to copy and paste is (1) print screen (2) paste the screen to the windows paint program (3) crop the waveform (4) paste it here.).



**Problem 2 (40 points)** Design a circuit that takes three bits A, B, S as input, and output one bit O as output. If S=0, O=A|B. If S=1, O=A&B.

(a) Construct the truth table.

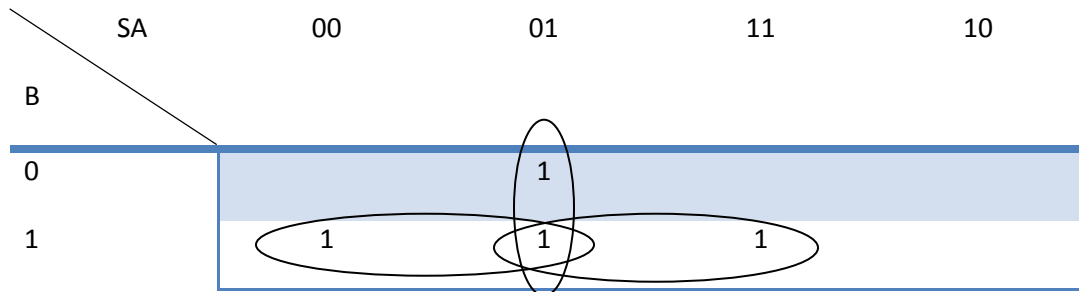
S	A	B	O
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0

1	1	1	1
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(b) Write down the sum-of-product form of the function without any simplification in the form as:  $O = (A \& B \& S) | (A \& B \& \sim S) | \dots$  (this is NOT the answer)

$$O = (\sim S \& \sim A \& B) | (\sim S \& A \& \sim B) | (\sim S \& A \& B) | (S \& A \& B)$$

(c) Simplify the circuit using K-map.



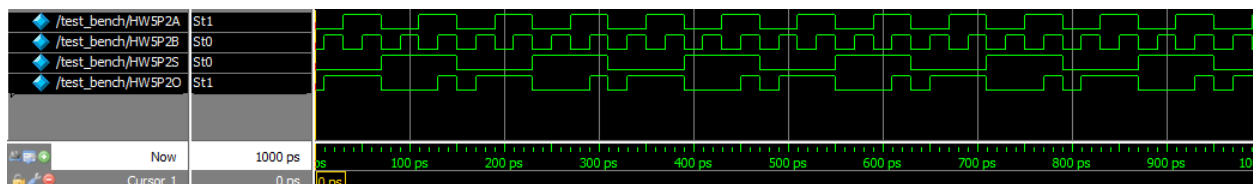
(d) Write down the Verilog module for this circuit called module HW5P2 (S,A,B,O).

```

module HW5P2 (S,A,B,O);
    input S, A, B;
    output O;
    assign O = (~S&A)|(A&B)|(~S&B);
endmodule

```

(e) \*\*\*\*A Verilog code has been provided for this homework with an empty HW5P2 module. Please replace this module with your module and run simulation. Copy and paste the waveform **only related to this problem** here. (One way to copy and paste is (1) print screen (2) paste the screen to the windows paint program (3) crop the waveform (4) paste it here.).



**Problem 3 (10 points)** Design a comparator which has 6 input bits, A2, A1, A0 and B2, B1, B0, and one output bit O. Let A=( A2, A1, A0) and B=(B2, B1, B0), and regard them as unsigned integers. If A>B, O=1; else O=0. **Please write down the logic function as your answer. No Verilog code or simulation is needed.** Hint: This problem should be solved by analyzing the underlying logic and no K-map is needed. For example, if A2=1 and B2=0, O must be 1 and there is no need to check the values of other input bits.

[Ans.] The key is the less significant bits matter only when the more significant bits are the same. So,

$$O = (A2 \& \sim B2) \mid (\sim(A2 \wedge B2) \& A1 \& \sim B1) \mid ((\sim(A2 \wedge B2) \& (\sim(A1 \wedge B1) \& A0 \& \sim B0))$$

**Problem 4 (10 points)** We talked about multiplexors in the class. A 4-1 multiplexor has 6 inputs: S1, S0, d3, d2, d1, and d0. It has one output, O. It works as follows. If S1S0=00, O=d0. If S1S0=01, O=d1. If S1S0=10, O=d2. If S1S0=11, O=d3. Show how to use only one 4-1 multiplexor (no any other gates should be used, including the inverter, meaning that the inputs to the 4-1 multiplexor can only come from A, B, C, 0, and 1) to implement function F(A,B,C) with truth table as follows. **Please finish the following figure, showing each input of the 4-1 multiplexor is connected to what input value, as your answer. No Verilog code or simulation is needed.** Hint: For this problem, no K-map is needed.

A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

[Ans.] Connect  $S1 \leftarrow A$ ,  $S0 \leftarrow B$ ,  $d3 \leftarrow 0$ ,  $d2 \leftarrow 1$ ,  $d1 \leftarrow C$ ,  $d0 \leftarrow 0$

