Assignment #6 – Digital Logic Design II – Sequential Logic

CDA 3100, Computer Organization I

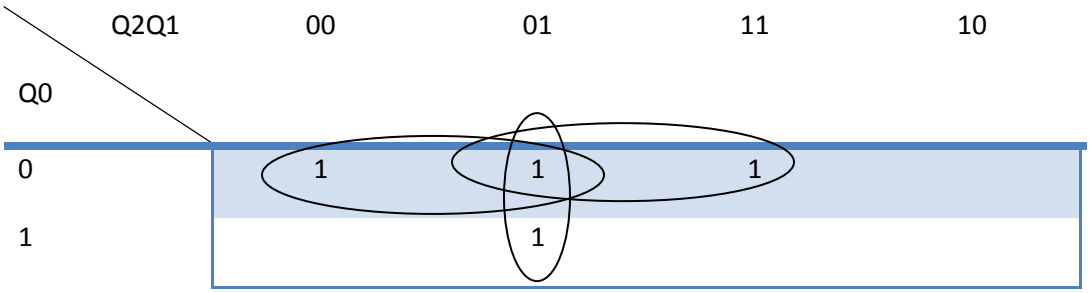
Problem 1 (50 points) Design a circuit that has an input clk, and an output Q which has three bits. At the rising edge of the clk, the unsigned binary number represented by Q changes according to the pattern: 04273651042736510…In other words, it starts with 0 and repeats 04273651 every 8 clock cycles.

(a) (10 points) Write down the next-state table.

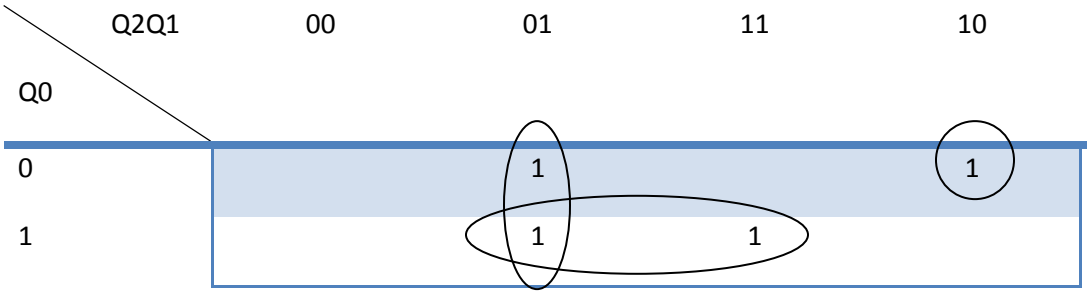
Q2	Q1	Q0	D2	D1	D0
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	1	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	1	0	1
1	1	1	0	1	1

(b) (10 points) Use Karnaugh map, derive the function for D2, D1, and D0.

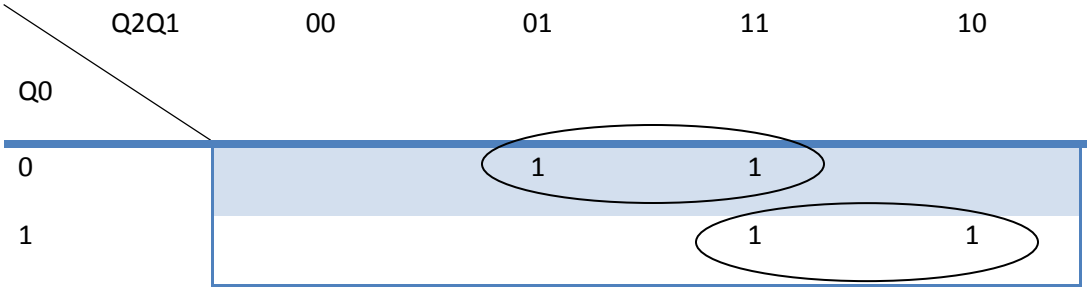
D2 =



D1 =



D0 =



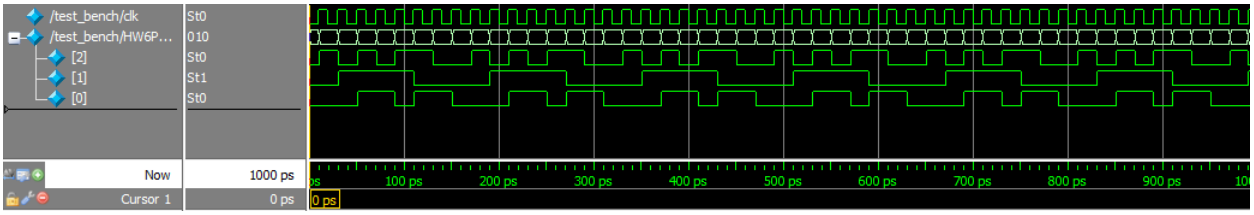
(c) (10 points) Write down a Verilog module for this circuit. Use the following code as a template.

module HW6P1 (clk, Q);

```
input clk;
output [2:0] Q;

wire Q2, Q2bar, Q1, Q1bar, Q0, Q0bar, D2, D1, D0;

assign D0 = (Q1 & ~Q0) | (Q2 & Q0);
Dff1 C0 (D0, clk, Q0, Q0bar);

assign D1 = (~Q2 & Q1) | (Q1 & Q0) | (Q2 & ~Q1 & ~Q0);
Dff1 C1 (D1, clk, Q1, Q1bar);

assign D2 = (~Q2 & ~Q0) | (Q1 & ~Q0) | (~Q2 & Q1);
Dff1 C2 (D2, clk, Q2, Q2bar);

assign Q[2] = Q2;
assign Q[1] = Q1;
assign Q[0] = Q0;
```

endmodule

(d) (10 points) Run the simulation, and show the waveform here. **Please only show the signals relevant to this problem.** That is, please show only the clock and Q as an unsigned (3-bit) number. Points will be taken off if this requirement is not satisfied.



(e) (10 points) Add one input "clr" to the circuit. If clr is 1, the circuit functions as previously. If "clr" is 0, Q is set to be 0 at the next rising edge. For this problem, just show the logic functions for D2, D1, and D0.

D2 = clr & (~Q2 & ~Q0) | (Q1 & ~Q0) | (~Q2 & Q1)

D1 = clr & (~Q2 & Q1) | (Q1 & Q0) | (Q2 & ~Q1 & ~Q0)

D0 = clr & (Q1 & ~Q0) | (Q2 & Q0)

Problem 2 (50 points) Design a circuit that has two inputs, clk and X, and produces one output O. X may change every clock cycle, and the change happens at the falling edge. The circuit samples the input at every rising edge of the clock. If the input is 1, consider as read a 1, else read a 0. O is 1 (for one clock cycle, from positive edge to positive edge) if the last three bits read are 100, with 0 as the most recent bit.

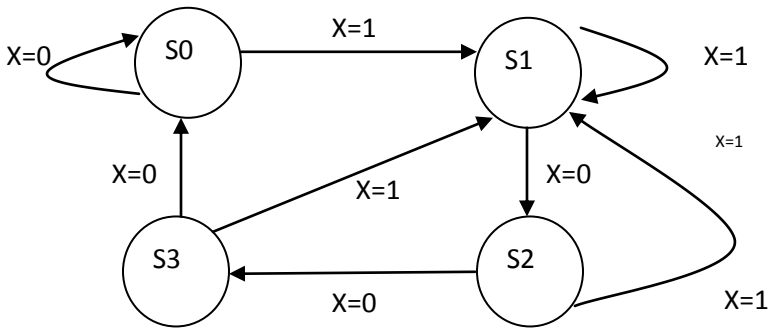
(a) (20 points) Draw the state diagram. Close to an arc, show X=1 or X=0 to indicate whether the change of state happens when X=1 or when X=0.

S0: got nothing

S1: got 1

S2: got 10

S3: got 100



(b) (10 points) Draw the next-state table, and derive the functions for D1 and D0. Derive the output function.

S0:00, S1:01, S2:10, S3:11.

Q1	Q0	X	D1	D0
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	1

O = Q1&Q0

D1 = (~Q1 & Q0 & ~X) | (Q1 & ~Q0 & ~X)

D0 = X | (Q1 & ~Q0)

(c) (10 points) Write down a Verilog module for this circuit. Use the following code as a template.

```
module HW6P2 (clk, X, O);
        input clk, X;
        output O;

        wire D1, D0, Q1, Q0, Q1bar, Q0bar;

        assign D0 = X | (Q1 & ~Q0);
        Dff1 C0 (D0, clk, Q0, Q0bar);

        assign D1 = (~Q1 & Q0 & ~X) | (Q1 & ~Q0 & ~X);
        Dff1 C1 (D1, clk, Q1, Q1bar);

        assign O = Q1&Q0;

endmodule
```

(d) (10 points) Run the simulation, and show the waveform here. **Please only show the signals relevant to this problem.** That is, please show only the clock, X and O. Points will be taken off if this requirement is not satisfied.