

Stephen R. Hines

CONTACT INFORMATION	2128 Wesley Ct. Tallahassee, FL 32303 phone: (352) 348-4401	citizenship: United States of America hines@cs.fsu.edu http://www.cs.fsu.edu/~hines
RESEARCH INTERESTS	Optimizing Compilers, Computer Architecture, Embedded Systems, Linkers	
EDUCATION	Florida State University , Tallahassee, Florida USA Ph.D. Computer Science, Expected August 2008 M.S. Computer Science, August 2004 Illinois Institute of Technology , Chicago, Illinois USA B.S. Computer Engineering, May 2001	
HONORS AND AWARDS	Florida State University : Graduate Student Research and Creativity Award, 2008 University Fellowship, 2006–2007 Computer Science Graduate Student Research Award, 2005 Harris Graduate Fellowship, 2003 Upsilon Pi Epsilon, 2003 Iowa State University : ECpE Graduate Excellence Fellowship, 2001–2002 Teaching Excellence Award, 2002 Illinois Institute of Technology : Camras/NEXT Scholarship, 1997–2001 Graduated High Honors in Computer Engineering, 2001	
ACADEMIC EXPERIENCE	Florida State University , Tallahassee, Florida USA <i>Graduate Student</i> Includes graduate level coursework and research. ◆ GPA: 4.0	August 2002 – present
	<i>Instructor</i> Developed and taught undergraduate course covering XHTML, PHP and Javascript. ◆ CGS 3066: Intro. to Internet Technology	January – May 2003
	<i>Teaching Assistant</i> Duties included developing, leading and grading weekly computer lab exercises. ◆ CGS 3408: Intro. to C Programming	August – December 2002
	Iowa State University , Ames, Iowa USA <i>Graduate Student</i> Includes graduate level coursework and research. ◆ GPA: 3.73	August 2001 – May 2002
	<i>Instructor</i> Taught undergraduate course in Computer Organization. ◆ CprE 305: Computer Organization and Assembly Language	January – May 2002
	<i>Teaching Assistant</i> Duties included developing, leading and grading weekly computer lab exercises. ◆ CprE 483: Hardware/Software Integration ◆ CprE 484: Advanced Digital Design	August – December 2001

Illinois Institute of Technology, Chicago, Illinois USA

Undergraduate Student

August 1997 – May 2001

Includes undergraduate level coursework and research.

◆ GPA: 3.944

Instructor

May – August 2001

Taught introductory graduate course in Data Structures and Algorithms in C++.

◆ CS 401: Data Structures and Algorithms

Teaching Assistant

January 2000 – May 2001

Duties included developing, leading and grading weekly computer lab exercises.

◆ CpE 101: Intro. to Computer Engineering

◆ CS 350: Computer Organization

◆ CS 470: Computer Architecture

◆ CS 471: Designing Computer Processors

RESEARCH
EXPERIENCE

Intel Corporation, Santa Clara, California USA

Graduate Research Intern

May 2006 - August 2006

Improved open-source Harmony JVM framework to support dynamic binary translation of native methods to an internal high-level representation suitable for leveraging existing optimizations.

Florida State University, Tallahassee, Florida USA

Research Assistant

May 2004 – present

Modified VPO compiler and SimpleScalar to support instruction packing with an IRF (Instruction Register File). Instruction packing is a joint compiler/architectural approach for reducing code size, energy consumption and execution time by placing the most frequently occurring instructions into a small bank of easily accessed registers. Designed and evaluated the TH-IC (Tagless Hit Instruction Cache), which improves the energy efficiency and performance of small caches by making guarantees about instruction fetch behavior.

Research Assistant

January 2002 – May 2004

Modified VPO compiler and developed ASM2RTL translator to assist in experimenting with de-optimization and re-optimization of assembly code.

Illinois Institute of Technology, Chicago, Illinois USA

Summer Researcher

May – August 2000

Modified the Linux kernel to support increased precision for timing measurements of processes and threads.

PUBLICATIONS *Ph.D./M.S. Research:*

1. **Stephen Hines**, David Whalley, and Gary Tyson. Guaranteeing hits to improve the efficiency of a small instruction cache. In *Proceedings of the 40th annual ACM/IEEE International Symposium on Microarchitecture (MICRO)*, pages 433–444. IEEE Computer Society, December 2007. [21.1% acceptance rate]
2. **Stephen Hines**, Gary Tyson, and David Whalley. Addressing instruction fetch bottlenecks by using an instruction register file. In *Proceedings of the 2007 ACM SIGPLAN conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, pages 165–174, June 2007. [27.6% acceptance rate]
3. **Stephen Hines**, David Whalley, and Gary Tyson. Adapting compilation techniques to enhance the packing of instructions into registers. In *Proceedings of the ACM/IEEE*

International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), pages 43–53, October 2006. [41% acceptance rate]

4. **Stephen Hines**, Gary Tyson, and David Whalley. Reducing instruction fetch cost by packing instructions into register windows. In *Proceedings of the 38th annual ACM/IEEE International Symposium on Microarchitecture (MICRO)*, pages 19–29. IEEE Computer Society, November 2005. [19.7% acceptance rate]
5. **Stephen Hines**, Gary Tyson, and David Whalley. Improving the energy and execution efficiency of a small instruction cache by using an instruction register file. In *Proceedings of the 2nd Watson Conference on Interaction between Architecture, Circuits, and Compilers (P=AC²)*, pages 160–169, September 2005. [44.7% acceptance rate]
6. **Stephen Hines**, Prasad Kulkarni, David Whalley, and Jack Davidson. Using de-optimization to re-optimize code. In *Proceedings of the 5th annual ACM International Conference on Embedded Software (EMSOFT)*, pages 114–123. ACM Press, September 2005. [28.4% acceptance rate]
7. **Stephen Hines**, Joshua Green, Gary Tyson, and David Whalley. Improving program efficiency by packing instructions into registers. In *Proceedings of the 2005 ACM/IEEE International Symposium on Computer Architecture (ISCA)*, pages 260–271. IEEE Computer Society, June 2005. [23.2% acceptance rate]

Other Research:

1. Chris Zimmer, **Stephen Hines**, Prasad Kulkarni, Gary Tyson, and David Whalley. Facilitating compiler optimizations through the dynamic mapping of alternate register structures. In *Proceedings of the ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pages 165–169, October 2007. [42.9% acceptance rate]
2. William Krehling, **Stephen Hines**, David Whalley, and Gary Tyson. Reducing the cost of conditional transfers of control by using comparison specifications. In *Proceedings of the 2006 ACM SIGPLAN conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, pages 64–71. ACM Press, June 2006. [25.3% acceptance rate]
3. Prasad Kulkarni, Wankang Zhao, **Stephen Hines**, David Whalley, Xin Yuan, Robert van Engelen, Kyle Gallivan, Jason Hiser, Jack Davidson, Baosheng Cai, Mark Bailey, Hwashin Moon, Kyunghwan Cho, and Yunheung Paek. VISTA: VPO interactive system for tuning applications. *ACM Transactions on Embedded Computing Systems (TECS)*, 5(4):819–863, 2006.
4. Matthew Kleffner, Douglas Jones, Jason Hiser, Prasad Kulkarni, Julie Parent, **Stephen Hines**, David Whalley, Jack Davidson, and Kyle Gallivan. On the use of compilers in DSP laboratory instruction. In *Proceedings of the 2006 IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, pages II 977–980, May 2006. [48.1% acceptance rate]
5. Prasad A. Kulkarni, **Stephen R. Hines**, David B. Whalley, Jason D. Hiser, Jack W. Davidson, and Douglas Jones. Fast and efficient searches for effective optimization phase sequences. *ACM Transactions on Architecture and Code Optimization (TACO)*, pages 165–198, June 2005.
6. Prasad Kulkarni, **Stephen Hines**, Jason Hiser, David Whalley, Jack Davidson, and Doug Jones. Fast searches for effective optimization phase sequences. In *Proceedings of the ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pages 171–182, June 2004. [19.5% acceptance rate]

- PATENTS ◆ **Lookahead Instruction Fetch**, co-inventors: David Whalley, Gary Tyson and Stephen Hines, U.S. Patent Pending, 2007.
- COMPUTER SKILLS ◆ Languages: C, C++, Python, VHDL, Lex, Yacc, Unix shell scripts and tools, Various Assembly (MIPS, ARM, PPC, SPARC, X86).
 ◆ Web: XHTML, PHP, Javascript.
 ◆ Applications: L^AT_EX, OpenOffice.org, M5, SimpleScalar, VPO, GNU binutils.
 ◆ Operating Systems: Unix/Linux (Gentoo), Windows.
- PROFESSIONAL ACTIVITIES *Program Committee*
 ◆ Workshop on Tools, Infrastructures and Methodologies for the Evaluation of Research Systems (TIMERS 2008)
Reviewer
 ◆ High Performance Computer Architecture (HPCA 2007)
 ◆ International Conference on Computer Design (ICCD 2007)
 ◆ Languages, Compilers and Tools for Embedded Systems (LCTES 2007)
 ◆ Compilers, Architecture and Synthesis for Embedded Systems (CASES 2006)
 ◆ International Symposium on Computer Architecture (ISCA 2006)
 ◆ Languages, Compilers and Tools for Embedded Systems (LCTES 2006)
 ◆ Workshop on Optimizations for DSP and Embedded Systems (ODES 2006)
 ◆ Programming Language Design and Implementation (PLDI 2005)
- REFERENCES Available upon request