Design a Sequential Circuit:

- Has two inputs, clk and X, and one output, O
- State based (uses a DFF)
- Output is 1 if the last three values of X (timed by the rising edge of clk) are 011 with 0 being the oldest value.

- Draw a state diagram to illustrate the circuit’s behavior.
Design a Sequential Circuit: State Diagram

Design a Sequential Circuit: State Diagram

X=1

X=0

X=1

X=0

X=1

X=0

X=1

X=0

S0

S1

S2

S3

S0

S1

S2

S3
Design a Sequential Circuit: Truth Table

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q0</th>
<th>X</th>
<th>D1</th>
<th>D0</th>
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<tbody>
<tr>
<td>0</td>
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Design a Sequential Circuit: 
K-Map for D1

D1 = (~Q1 & Q0 & X) | (Q1 & ~Q0 & X)
Design a Sequential Circuit: K-Map for D0

\[ D0 = \sim X \mid (Q1 \& \sim Q0) \]
module seqdector(clk, X, O);
    input clk, X;
    output O;
    wire D1, D0, Q1, Q0, Q1bar, Q0bar;
    assign D0 = ~X | (Q1 & ~Q0);
    Dff1 C0(D0, clk, Q0, Q0bar);
    assign D1 = (~Q1 & Q0 & X) | (Q1 & ~Q0 & X);
    Dff1 C1(D1, clk, Q1, Q1bar);
    assign O = Q1 & Q0;
endmodule